

PCB LAYOUT OPTIMISATION

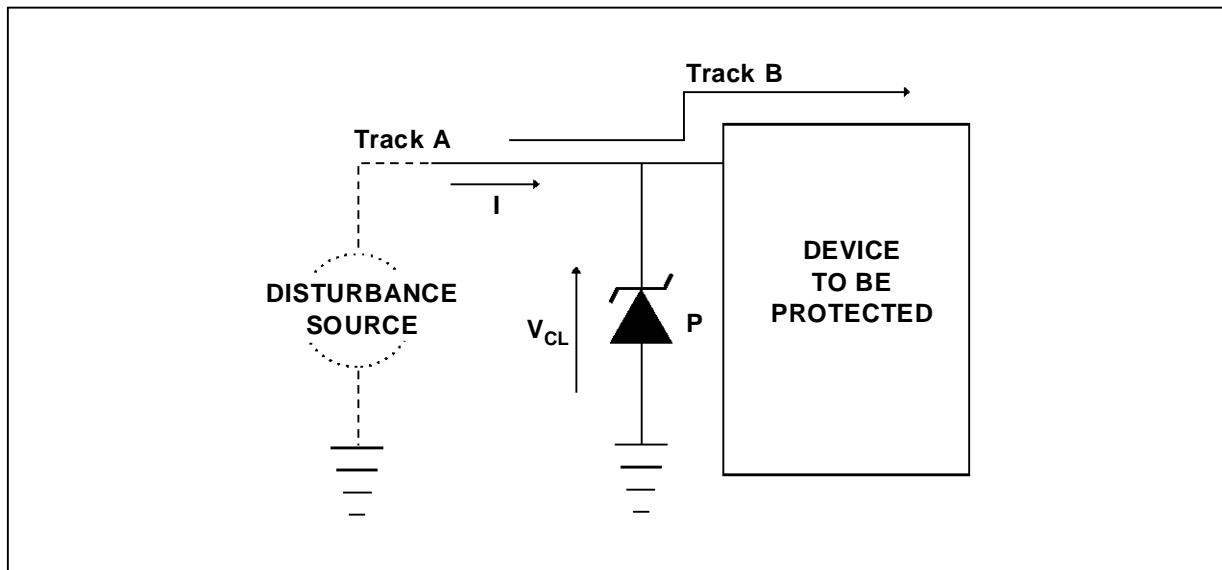
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1. INTRODUCTION

Protection requirements are becoming more and more well known and are often defined by rules or standards. To satisfy these requirements, there is, in the majority of cases, a standard solution or a dedicated product.

However, knowledge of the disturbances and the use of suitable protection devices are not sufficient in themselves to solve the problem. In many applications, the correct design of the PCB layout is essential for success.

Figure 1 : Classical protection location

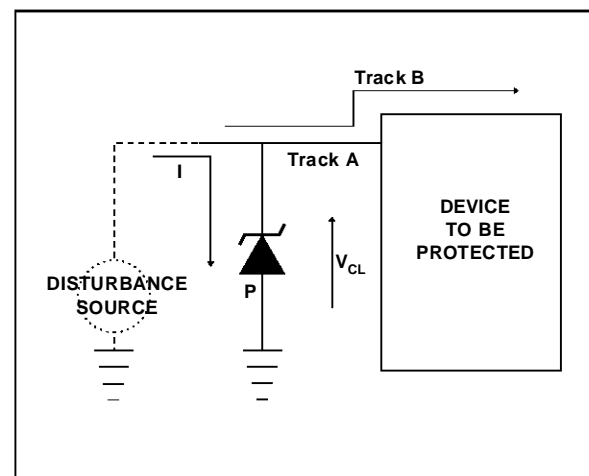


2. INFLUENCE OF THE PROTECTION LOCATION

The circuit presented in figure 1 shows the classical approach for the protection location. Here the protection device * is located close to the module to be protected. When a disturbance occurs on the track A the TRANSIL P clamps the surge at a maximum voltage V_{CL} and thus protects the sensitive part.

During this clamping action there is a current through P and also in the track A. This phenomenon induces a voltage on track B, where it is close to A. To avoid this undesirable parasitic overvoltage on track B, the circuit of figure 2 is recommended.

Figure 2 : Recommended protection location



APPLICATION NOTE

In this case the current due to the clamping phase of P remains located in the disturbance area and the track B is not affected.

To summarize, it is recommended that the protection device is located as close as possible the disturbance source. For example, all the lines coming into the board ought to be protected close to the connector.

3. INFLUENCE OF THE PCB LAYOUT ON THE ESD PROTECTION

These days, printed circuit boards are often auto-routed by computer aided design and the track lengths are not optimized.

Figure 3 : Non-optimized LAYOUT for ESD

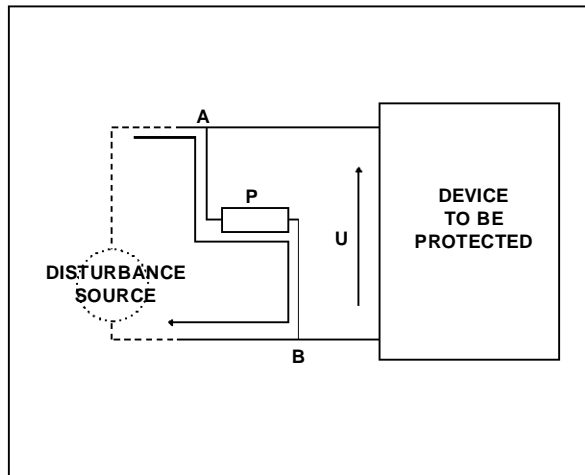
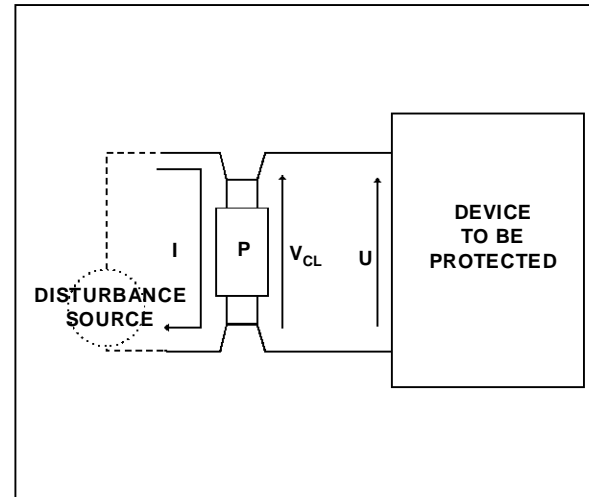


Figure 3 shows the classical non-optimized layout. When a surge occurs the protection device P acts and there is a clamping voltage V_{CL} across it. Due to the fast rise time of the ESD overvoltage there is a high di/dt between the points A and B. This di/dt generates, in the parasitic inductances located between A and P and between B and P, overvoltages up to several hundred volts. So the applied voltage V across the device to be protected is the sum of the clamping voltage and the voltage across the parasitic inductance : thus the sensitive module is not protected.

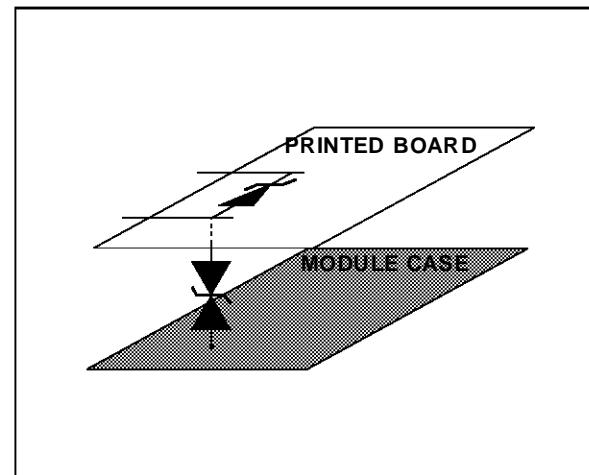
In the case of figure 4, the design topology is based on a 4 point circuit. When a surge occurs the Transil clamps at V_{cl} and due to the design the di/dt effects remain on the left hand side of P. Therefore the voltage V seen by the sensitive device is roughly equal to V_{CL} .

Figure 4 : Optimized layout for ESD



N.B. : The surface mount family SOD6 and SOD15 are particularly suited to this kind of application.

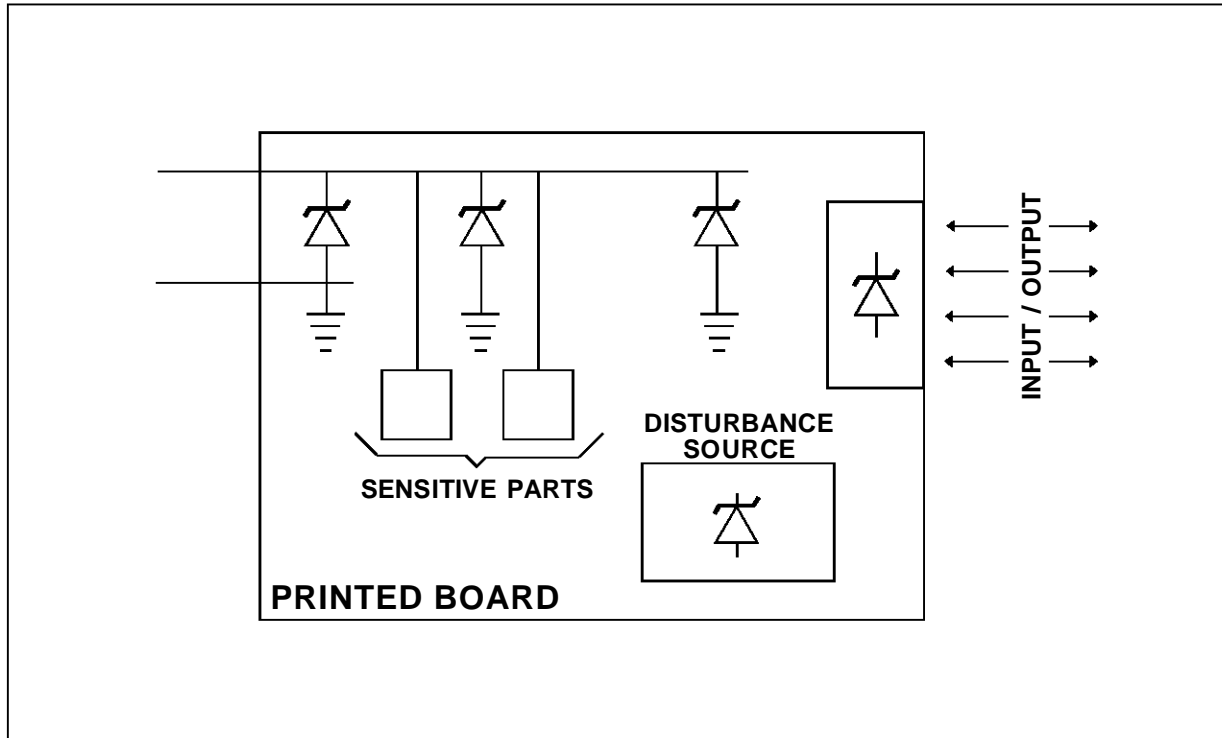
Figure 5 : Printer circuit board protection against ESD with case



These days most inputs are protected against ESD (though not always effectively) and so the voltage between the lines and ground never exceeds dangerous values.

However, this does not prevent the total electrical potential from increasing, possibly resulting in sparks between one point of the board and the module case. To avoid this problem we recommend a bidirectional Transil (BZW04P37B) between the printed circuit board ground and the metallic parts of the case.

Figure 6 : Distributed protection



4. DISTRIBUTED PROTECTION

The printed circuit board shown in figure 5 represents a general case. In this board the input/output lines are protected close to the connector and overvoltages are cancelled close to the disturbance sources. The other lines to be protected are the power supply wires which carry 3 kinds of disturbances :

- The overvoltages resulting from mains perturbations.
- The surges coming from the other boards supplied by these lines.
- The disturbances generated on the board by the normal operation of the resident module, for example the di/dt due to the fast switching of a buffer.

To suppress these surges we suggest a powerful Transil (1.5 KE for example) close to the power supply input on the board, and some lower power devices (e.g. BZW04) distributed around the board area.

5. CONCLUSION

Due to the parasitic inductance of PCB tracks, a protection device chosen purely according to disturbance standards does not assure immunity from surges. Carefully designed PCB layout plus correct device selection from the SGS-THOMSON range is essential to guarantee adequate protection.

* TRANSIL devices are used as examples throughout this document, but the same arguments are valid for TRISILS.

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